REMARKS

Claims 1-20 are pending in the present application. Claims 1, 3, 4, 9, 11, 12, 16 and 18 have been amended.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the Priority Document.

Claim Rejections-35 U.S.C. 103

Claims 1-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Weber et al. reference (U.S. Patent No. 6,242,789) in view of Japanese Patent Publication No. 4-348517. This rejection is respectfully traversed for the following reasons.

The Examiner has acknowledged that claims 4 and 8 include allowable subject matter, and thus would be allowable if rewritten in independent form. Accordingly, claims 4 and 8 should not be included as rejected under 35 U.S.C. 103. **The Examiner is therefore respectfully requested to confirm the status of claims 4 and 8.**

The semiconductor device of claim 1 includes in combination a dielectric sidewall structure "formed on the side face of the through hole so that the dielectric sidewall structure gradually narrows the through hole"; and a fuse "formed of a conductive material that buries the narrowed through hole, said fuse having a lower end connected

to the first conductive layer and an upper end connected to the second conductive layer". Applicant respectfully submits that the semiconductor device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

The Examiner has primarily relied upon the Weber et al. reference, acknowledging that the sidewalls within fuse hole 102 are not gradually narrowed. In order to overcome this acknowledged deficiency, the Examiner has relied upon Japanese Patent Publication No. 4-348517 as disclosing a contact hole with a polycrystalline semiconductor sidewall that narrows the hole towards the base of the hole, as illustrated in Figs. 7 and 12. The Examiner has alleged that it would have been obvious to include the required hole narrowing in the Weber et al. reference in view of Japanese Patent Publication No. 4-348517, in order to have a semiconductor device with increased performance. Applicant respectfully disagrees for the following reasons.

As acknowledged by the Examiner, Japanese Patent Publication No. 4-348517 discloses a conductive sidewall in the contact hole. The following is an English translation of a pertinent portion of Japanese Patent Publication No. 4-348517:

> "[0016] [Effect of the Invention] A contact hole formed by a method of the present invention has a proper taper at a sidewall of the contact hole in the direction of easy flow by a conductive sidewall."

Accordingly, as mentioned above, the contact hole in Japanese Patent Publication No. 4-348517 is filled with two conductive materials. The first material is polysilicon that

forms a sidewall, and the second material is a metal such as aluminum.

As described beginning in column 6, line 14 of the Weber et al. reference with respect to Fig. 14 as relied upon by the Examiner, fuse hole 102 includes a CVD aluminum wetting layer 114 on a liner material layer 104 such as stacked implanted titanium and/or a CVD TiN. Accordingly, fuse hole 102 in Fig. 14 of the Weber et al. reference includes first and second conductive layers thereon.

In contrast, the semiconductor device of claim 1 as noted above includes a dielectric sidewall structure formed on the side face of the through hole, so that the dielectric sidewall structure gradually narrows the through hole. The prior art as relied upon by the Examiner clearly fails to meet these features of claim 1, because the sidewalls in the Weber et al. reference and Japanese Patent Publication No. 4-348517 are conductive layers, not dielectric. The through hole of claim 1 is narrowed by a dielectric sidewall structure and filled with a conductive material, to provide a fuse having a desired shape. Applicant therefore respectfully submits that the semiconductor device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 1-3 and 5-7, is improper for at least these reasons.

The semiconductor device of claim 9 includes in combination a dielectric sidewall structure "formed on a side surface of the through hole so that the dielectric sidewall structure gradually narrows the through hole". The semiconductor device of claim 16 includes in combination a dielectric sidewall structure "formed in the through

hole so that the through hole is gradually narrowed by the dielectric sidewall structure to expose the first conductive film".

As noted above, the Weber et al. reference and Japanese Patent Publication No. 4-348517 do not include a dielectric sidewall structure within a through hole. Applicant therefore respectfully submits that the semiconductor devices of respective claims 9 and 16 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 9-20, is improper for at least these reasons.

Allowable Subject Matter

Applicant respectfully notes the Examiner's acknowledgment that claims 4 and 8 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Applicant however respectfully submits that claims 4 and 8 should be considered allowable by virtue of dependency upon claim 1, and that amendment of claims 4 and 8 to be in independent form is therefore unnecessary.

Conclusion

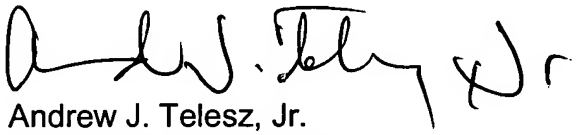
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740